PATENT

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September 8, 2005 — Phoebe E. Pogson

Date — Phoebe E. Pogson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 09/998,594	Confirmation No.	: 6204
Applicant	: Leland R. Nevill		
Filed	: November 16, 2001	Attorney Docket No.	: 500060.02
Art Unit	: 2876	Customer No.	: 27,076
Examiner	: Daniel St. Cyr		
Title	: METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS		

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APPELLANT'S BRIEF (37 C.F.R. § 1.192)

Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on January 14, 2004 and the Notification of Non-Compliant Appeal Brief dated August 8, 2005. The fees required under Section 1.17(c), and any required request for extension of time for filing this brief and fees therefor, are dealt with in the accompanying transmittal letter.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc., a Delaware Corporation having a principal place of business at Boise, Idaho.

II. RELATED APPEALS AND INTERFERENCES (IF ANY)

There are no other appeals or interferences known to appellant, the appellant's legal representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-34 are pending in this application. All of these claims have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,957,512, to Beffa in view of U.S. Patent No. 5,962,834 to Markman. Applicant is appealing from the rejections of all of these claims. Claims 1-34 were also rejected under 35 U.S.C. § 251 as being based on a defection reissue declaration. Applicant does not disagree with this rejection, but requested that it be held in abeyance until allowance pursuant to 37 CFR 1.111(b) and MPEP 714.02.

IV. STATUS OF AMENDMENTS

No amendment to the claims has been filed subsequent to the final rejection. The final rejection objected to the

V. SUMMARY OF INVENTION

The present invention is directed to an improved method an apparatus for identifying integrated circuits. Typically, a large number of identical integrated circuits or "dies" are fabricated on a single wafer of semiconductor substrate. After fabrication, a series of tests is performed and the test data are collected for each die. This test data may be used in subsequent assembly/packaging steps to ensure that only properly functioning die are packaged as integrated circuits. To correlate the various test results with the appropriate die, accurate identification of each die is required, both before and after packaging as an integrated circuit.

Many of today's integrated circuits have electronically readable identification information that is programmed into the integrated circuit itself. Also, ink or laser-scribed marks may be placed on either the die or on an external surface of a package in which the integrated circuit die will be housed. These marks typically indicate information such as date and country of manufacture, product and package types, speed or other test parameters, or manufacturing lot identification.

There are a number of problems with the current practices used to electronically program integrated circuits with identifying information and place optically readable markings on the integrated circuits. For example, the optical markings typically are not associated with the electrically programmed identifying information so that the optical markings do not uniquely identify each integrated circuit die or even each wafer in which the die was fabricated. As a result, obtaining information that uniquely identifies the particular die within the integrated circuit package typically requires special test apparatus. Furthermore, it is possible in some cases for the optical markings and/or the electrically programmed identifying information to be altered, possibly for improper purposes.

The subject matter of this appeal involves methods of identifying integrated circuits, integrated circuits, and wafers containing integrated circuits. As summarized more fully below, the identifying method involves electrically programming the integrated circuits with identifying information associated with the optical markings to provide significantly greater security than is provided than the prior art approaches described above. Even if an unauthorized person can electrically reprogram the identifying information and even if that unauthorized person can alter the optical markings, doing so will be of little value unless the unauthorized person knows which optical markings correspond to which the electrically programmed identifying information. However, this correlation can be provided by a lookup table, which can remain confidential. After the electrically programmed identifying information is read, the lookup table accessed to associate the electrically programmed identifying information with the optical markings. Alternatively, the optical markings are read, and the lookup table accessed to associate the optical markings with the electrically programmed identifying information.

The subject matter to which the independent claims involved in this appeal are directed will now be summarized with reference to the specification by page and line number and to the drawings, if any, by reference characters. However, it should be understood that these references to the specification and drawings do not limit the claims since the specification and drawings disclose only one of several examples of devices that are covered by each of the independent claims.

Claim 1 is directed to a method of identifying a plurality of substantially identical integrated circuits [10, Figures 1 and 2] formed on a common substrate. Each of the integrated

circuits [10, Figures 1 and 2] is programmed with respective electronic identification information [12, Figure 1] distinguishing the integrated circuits from one another [Col. 2, ll. 42-57, col. 3, ll. 33-35]. Each of the integrated circuits [10, Figures 1 and 2] is also marked with a respective optical identification code [14, Figures 1 and 2] which corresponds with the respective electronic identification information [Col. 2, l. 62-col. 3, l. 4]. The optical identification code [14, Figure 1] on each of the integrated circuits [10, Figures 1 and 2] is then subsequently read [Col. 3, ll. 4-11]. Finally, a lookup table is accessed to associate the optical identification code [14, Figures 1 and 2] on each of the integrated circuits [10, Figures 1 and 2] with the corresponding electronic identification information [12, Figure 1] [Col. 3, ll. 43-48].

Claim 6 is directed to a method of identifying substantially identical integrated circuits [10, Figures 1 and 2] formed on a common substrate [16, Figure 2] in which each of the integrated circuits [10, Figures 1 and 2] include a programmable circuit [12, Figure 1] for storing respective electronically readable identification code, which distinguishes the integrated circuits [10, Figures 1 and 2] from one another. In accordance with the method, each of the integrated circuits [10, Figures 1 and 2] is marked with respective optical identification code [14, Figure 1] [Col. 2, l. 62-col. 3, l. 4]. A lookup table is then accessed to associate the optical identification code [14, Figures 1 and 2] on each of the integrated circuits [10, Figures 1 and 2] with the respective electronically readable identification code [12, Figure 1] [Col. 3, ll. 43-48]. Finally, the optical identification code [14, Figure 1] on each of the integrated circuits [10, Figures 1 and 2] is read [Col. 3, ll. 4-11].

Claim 10 is directed to a wafer [16, Figure 2] comprising a plurality of dies [18, Figure 2], each of which includes an integrated circuit [10, Figures 1 and 2] [Col. 3, ll. 11-15]. Each integrated circuit [10, Figures 1 and 2] has a programmable identification circuit [12, Figure 1] that stores identification data [Col. 2, ll. 42-57; col. 3, ll. 33-35]. Each die also has an optical identification mark [14, Figures 1 and 2] positioned thereon and encoding information corresponding to the identification data [Col. 2, l. 62-col. 3, l. 4]. The optical identification mark [14, Figures 1 and 2] on each die [18, Figure 2] is accessed through a lookup table to correspond to the electronic identification information [Col. 3, ll. 43-48].

Claim 14 is directed to integrated circuit chips [10, Figures 1 and 2], each of which includes a housing [20, Figure 3] [Col. 3, ll. 19-23]. An integrated circuit [10, Figures 1

and 2] enclosed within the housing [20, Figure 3] and including an identification circuit [12, Figure 1] that stores identification data distinguishing each of the integrated circuit chips from one another [Col. 2, ll. 42-57, col. 3, ll. 33-35]. An optical mark [14B, Figure 3] is positioned on an exterior surface of the housing [20, Figure 3] to encode identification information [Col. 2, l. 62-col. 3, l. 4]. The identification information encoded in the optical mark [14B, Figure 3] is accessed through a lookup table to correspond to the identification data [12, Figure 1] [Col. 3, ll. 43-48].

Claim 19 covers a method of identifying a plurality of substantially identical integrated circuits [10, Figures 1 and 2] formed on a common substrate [16, Figure 2]. Each of the integrated circuits [10, Figures 1 and 2] are formed on a respective one of a plurality of substrate dies [18, Figure 2]. The method of claim 19 includes programming each of the plurality of integrated circuits [10, Figures 1 and 2] with respective electronic identification information [12, Figure 1] for each of the integrated circuits [Col. 2, ll. 42-57, col. 3, ll. 33-35]. Each of the integrated circuits [10, Figures 1 and 2] is also marked with a respective optical identification code [14, Figure 1] which corresponds with the respective electronic identification information [Col. 2, l. 62-col. 3, l. 4]. The optical identification code [14, Figure 1] on each of the integrated circuits [10, Figures 1 and 2] is then subsequently read [Col. 3, ll. 4-11]. Similarly, the electronic identification information [12, Figure 1] is also read from each of the integrated circuits [10, Figures 1 and 2] [Col. 2, ll. 52-61]. A lookup table is then accessed to associate the optical identification code [14, Figure 1] on each of the integrated circuits [10, Figures 1 and 2] with the corresponding electronic identification information [12, Figure 1] [Col. 3, ll. 43-48].

Claim 23 is directed to a method of identifying an integrated circuit [10, Figures 1 and 2] in which the integrated circuit [10, Figures 1 and 2] is programmed with an electronic identification information [12, Figure 1] [Col. 2, ll. 42-57, col. 3, ll. 33-35]. Each of the integrated circuits [10, Figures 1 and 2] is also marked with a respective optical identification code [14, Figures 1 and 2] which corresponds with the respective electronic identification information [Col. 2, l. 62-col. 3, l. 4]. The electronic identification information is then read [Col. 3, ll. 4-11], and the read electronic identification information is cross-referenced to the optical identification code [14, Figures 1 and 2] to associate the optical identification code [14, Figures 1

and 2] with the corresponding electronic identification information [12, Figure 1] [Col. 3, ll. 43-48].

Claim 28 is directed to an integrated circuit [10, Figures 1 and 2] including a programmable circuit [12, Figure 1] for storing an electronically readable identification code that identifies the integrated circuit[10, Figures 1 and 2] [Col. 2, ll. 42-57, col. 3, ll. 33-35]. The method of claim 28 includes marking the integrated circuit [10, Figures 1 and 2] with an optical identification code [14, Figures 1 and 2] which corresponds with the respective electronic identification information [Col. 2, l. 62-col. 3, l. 4]. The electronically readable identification code [12, Figure 1] is then read [Col. 3, ll. 4-11], , and the read electronically readable identification code is compared to the optical identification code [14, Figures 1 and 2] to associate the optical identification code [14, Figures 1 and 2] with the corresponding electronically readable identification code [12, Figure 1] [Col. 3, ll. 43-48].

The final independent claim involved in this appeal is claim 32. Claim 32 is directed to an integrated circuit [10, Figures 1 and 2] comprising an integrated circuit chip [18, Figure 2] mounted within a package [20, Figure 3] [Col. 3, ll. 19-23]. The claim integrated circuit [10, Figures 1 and 2] includes an identification circuit [12, Figure 1] fabricated on the integrated circuit chip [18, Figure 2] to store identification data [Col. 2, ll. 42-57, col. 3, ll. 33-35]. An optical identification mark [14B, Figure 3] on the package [20, Figure 3] of the integrated circuit [10, Figures 1 and 2] encodes information corresponding to the identification data [Col. 2, l. 62-col. 3, l. 4].

VI. ISSUES

1. Does 35 U.S.C. § 103(c) preclude using U.S. Patent No. 5,957,512 to Beffa to support a rejection under 35 U.S.C. § 103(a)?

2. If the patent to Beffa can be used to support an obviousness rejection, would claims 1-34 have been considered obvious over the patent to Beffa in view of U.S. Patent No. 5,962,834 to Markman?

VII. GROUPING OF CLAIMS

The claims do not stand or fall together. For purposes of this appeal, claims 1-31 can be grouped together, and claims 32-34 can be grouped together.

VIII. ARGUMENTS

1. 35 U.S.C. § 103(c) Precludes Using U.S. Patent No. 5,957,512 To Support A Rejection Under 35 U.S.C. § 103(a)?

Under 35 U.S.C. § 103(c), "[s]ubject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person." The Beffa patent qualifies as prior art only under one or more of subsections (e), (f), and (g) of Section 102. Both the Beffa patent and the present application are assigned to the same assignee, namely Micron Technology, Inc. The undersigned states as follows regarding the common ownership of the Beffa patent and the invention covered by the present patent application:

> Statement Regarding Common Ownership
>
> The Beffa patent and the invention covered by the present patent application were, at the time the invention covered by the present application was made, subject to an obligation of assignment to Micron Technology, Inc., which is the assignee of the present application and the Beffa patent.

The exclusion from prior art provided by 35 U.S.C. § 103(c) "applies to all utility, design and plant patent applications filed on or after November 29, 1999, including continuing applications filed under 37 CFR 1.53(b), continued prosecution application filed under 37 CFR 1.53(d), and **reissues**. [*See,* MPEP 706.02(l)(1), emphasis added]. Accordingly, the Beffa patent may not be applied as prior art under Section 103 against the claims of the present application.

2. Claims 1-34 Would Not Have Been Obvious Over The Patent To Beffa In View Of The Patent To Markman

A. The Subject Matter Disclosed In The Beffa Patent

The Beffa patent discloses a method for sorting integrated circuit devices in which a unique identification code is programmed into each of the integrated circuit devices. The identification code can be used during manufacture and test for a variety of purposes, such as sorting the integrated circuits based on reliability, manufacturing process recipe, etc. However, the Beffa patent does not disclose or suggest providing any optically viewable markings to an integrated circuit. Nor does the Beffa patent disclose or suggest any reasons or motivations to add optical markings to an integrated circuit that has been electrically programmed with identifying information.

The Office Action states that the Beffa patent "teaches that code could be read optically," citing Figure 8 and column 7, line 8+. However, as admitted by the Examiner, the Beffa patent does not teach or fairly suggest *both* applying optically readable identification marks to the integrated circuit *and* also electronically programming the integrated circuit with identifying information; and particularly not optical identification information that has been correlated with the electrically programmed identification information.

B. The Subject Matter Disclosed In The Markman Patent

The patent to Markman discloses a system for tracking and managing an inventory of clothing. A tag is placed on a hanger for each article of clothing. The tag has a bar code printed on its outer surface, and an RF transponder is embedded in the tag. When interrogated, the RF transponder transmits a coded RF signal. However, the information provided by the RF code and the bar code are not correlated to each other. Instead, both of them are separately associated with the article of clothing. (*See, e.g.*, column 9, line 6-7 "the packet 14 is associated with the trackable unit"). The Markman patent does not teach or fairly suggest associating the information in the RF code with the information provided by the bar code. Finally, the Markman patent does not suggest any other used for the disclosed clothing tags, nor does it suggest using an RF transponder and a bar code or other optically coded marking on or in an integrated circuit.

C. There Is No Suggestion To Combine Beffa With Markman

"When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references." *Akamai Technologies, Inc. v. Cable & Wireless Services, Inc.*, 344 F.3d 1186, 68 USPQ2d 1186 (Fed. Cir. 2003). The prior art does not suggest or disclose any motivation to combine the teachings in the Beffa patent with the teaching in the Markman patent. For example, the Beffa patent does not disclose any shortcomings in the disclosed programming of integrated circuits with identifying information that would motivate one skilled in the art to seek out the teachings of Markman. Nor does Markman disclose any reason why one skilled in the art would contemplate using the disclosed inventory tracking system or clothing label for integrated circuits.

D. The Markman Patent Is Non-Analogous Prior Art

The Markman patent is clearly non-analogous art which may not be used as a reference to reject the claims on grounds of obviousness. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of Applicant's endeavor, or if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oeitikar* 177 F.2d 1493, 1446 (Fed, Cur 1992). The Markman patent is neither.

The Markman patent is in the field of inventory tracking systems for clothing whereas Applicant's invention is in the field of integrated circuits, and, in particular, identifying semiconductor dies either electrically or visually after manufacture so test results can be properly correlated with the die. There is very little if any relationship between the field of inventory tracking and the field of integrated circuits.

The Markman patent is also not reasonably pertinent to the problem addressed by the subject matter of the claims. The problem addressed by Markman is keeping track of a large number of clothing items in inventory. The problem addressed by Applicant is being able to identify a particular semiconductor die both before and after packaging "in order to properly correlate the various test results with the appropriate die or dies" [Col. 1, lines 28-29]. The problem with identifying the semiconductor die is that "the electronically readable identification information is usually available only during those manufacturing procedures in which the integrated circuit is electrically tested." [Col. 1, lines 48-50]. As a result, the semiconductor die

cannot be identified after packaging, thereby preventing test results from being correlated with the integrated circuit. Applicant is not concerned with the inventory management problem addressed by Markman, *e.g.*, keeping track of the location of integrated circuits or determining how may integrated circuits are in inventory. The Markman patent therefore addresses a problem that is entirely different from the problem addressed by applicant.

Still another test of whether prior art is non-analogous is whether the inventor would logically have turned to the prior art field for guidance in solving the problem addressed by the invention. "A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, if it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem." *In re Clay*. 966 F.2d 656, 659 (Fed. Cir. 1992). There is absolutely no reason to believe that a semiconductor engineer faced with the problem of correlating test results with a semiconductor die both before and after packaging would have turned to the art of clothing inventory tacking systems for guidance. No testing or semiconductor die is involved in the Markman invention, and Applicant's invention is not involved with keeping track of the location or number of integrated circuits. Therefore, under any of the criteria that the Federal Circuit has used to determine if a prior art reference is analogous prior art, the Markman patent must be considered non-analogous prior art. For this reason, the Markman patent cannot support an obvious rejection of claim 1-34.

E. Claims 1-31 Would Not Have Been Obvious Over The Beffa Patent In View Of The Markman Patent

Claim 1-22 of U.S. Patent No. 5,984,190 and claims 23-31 of this reissue application specify a method of identifying integrated circuits, an integrated circuit or a wafer containing integrated circuits. Claim 1 will be considered representative of the claims in this group. Claim 1 specifies a method of identifying integrated circuits formed on a common substrate in which each of the integrated circuits is programmed with respective electronic identification information. This electronic identification information distinguishes the integrated circuits from each other. Claim 1 also specifies marking each of the integrated circuits with respective optical identification code, "which corresponds with the respective electronic identification information." As explained above, none of the cited references teach or suggest

both electronically programming an integrated circuit with electronic identification information and marking the integrated circuit with corresponding optical identification code.

Claim 1 further specifies reading the optical identification code and "accessing a lookup table to associate the optical identification code on each of the integrated circuits with the corresponding electronic identification information." Thus, claim 1 requires that the optical identification code be read, and used to look up the corresponding electronic identification information. The Beffa patent teaches only electronic identification information or optical markings, but not both. Therefore, it cannot teach reading one code and then using that code to reference the other. While the Markman patent discloses a tag having both electronic identification information and optical identification information, the patent indicates that only one type of information is used at a time. Specifically, the Markman patent states in lines 55-61 of column 6 "[a]ccording to an inventive aspect, the human and machine readable indicia provide alternative identification possibilities. For example, a business can have RF readers at some locations, barcode scanners at other locations, and can have manual data entry devices at additional locations for use if the automatic identification elements or the inventory control computer should fail" Therefore rather than teaching the use of one type of identification information to access the other as recited in the claims, the Markman patent teaches just the opposite, *i.e.*, using the two types of identification information alone as alternatives to each other.

Furthermore, neither of the cited references suggest that optical identification code should be associated with electronic identification information as recited in the claims, and they certainly do not disclose or suggest using a lookup table for this purpose. Although the computer system described in the Markman patent does use a lookup table, it uses that table to associate each type of individual identification information with the particular article of clothing. It does not teach using the lookup table to associate the two types of information with each other. For example, the Markman patent does not disclose a lookup table correlating the RF identification means 12 with the visual identification means 18. Claim 1-31 are therefore clearly patentable over the cited references.

F. Claims 32-32 Would Not Have Been Obvious Over The Beffa Patent In View Of The Markman Patent

Claim 32 is directed to an integrated circuit chip mounted within a package. An identification circuit is fabricated on the integrated circuit chip and is operable to store identification data. An optical identification mark is also placed on the package of the integrated circuit. Significantly, the optical identification mark encodes information corresponding to the identification data. As explained earlier, while the Markman patent may disclose RF identification means and visual identification means on the same packet or label, it does not disclose placing the packet in an integrated circuit. Nor does the Markman patent suggest using an optical identification mark to encode information corresponding to identification information stored in the identification circuit of an integrated circuit chip. For these reasons, claims 32-34 are patentable over the Beffa patent in view of the Markman patent.

IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

Attached hereto is a copy of pending claims 1-34, which are involved in this appeal.

Respectfully submitted,

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EWB:pep

Enclosures:
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APPENDIX

1. A method of identifying a plurality of substantially identical integrated circuits formed on a common substrate, comprising the steps of:

programming each of the integrated circuits with respective electronic identification information distinguishing the integrated circuits from one another; and

marking each of the integrated circuits with respective optical identification code which corresponds with the respective electronic identification information;

reading the optical identification code on each of the integrated circuits; and

accessing a lookup table to associate the optical identification code on each of the integrated circuits with the corresponding electronic identification information.

2. The method of claim 1 wherein the step of programming each of the integrated circuits with electronic identification information includes the step of programming one of a plurality of programmable links.

3. The method of claim 1 wherein the step of marking each of the integrated circuits with optical identification code includes the step of placing an adhesive label on each of the integrated circuits.

4. The method of claim 1 wherein the step of marking each of the integrated circuits with optical identification code includes the step of inscribing a symbol on each of the integrated circuits.

5. The method of claim 1 wherein the step of marking each of the integrated circuits includes the step of marking respective portions of the substrate on which the integrated circuits are formed.

6. In a plurality of substantially identical integrated circuits formed on a common substrate, each of the integrated circuits including a programmable circuit for storing

respective electronically readable identification code which distinguishes the integrated circuits from one another, a method of identifying the integrated circuits, comprising the steps of:

marking each of the integrated circuits with respective optical identification code;

accessing a lookup table to associate the optical identification code on each of the integrated circuits with the respective electronically readable identification code and

reading the optical identification code on each of the integrated circuits.

7. The method of claim 6 wherein the step of associating the optical identification code on each of the integrated circuits with the respective electronically readable identification code includes the steps of:

reading the electronically readable identification code stored in each of the integrated circuits;

reading the optical identification code marked on each of the integrated circuits; and

correlating the read electronically readable identification code with the read optical identification code for each of the integrated circuits.

8. The method of claim 6 wherein the step of associating the optical identification code on each of the integrated circuits with the respective electronically readable identification code includes the step of encoding identical data in the optical and electronically readable identification codes.

9. The method of claim 6 wherein the step of marking each of the integrated circuits includes the step of marking respective portions of the substrate on which the integrated circuits are formed.

10. A wafer comprising a plurality of dies, each die including an integrated circuit having a programmable identification circuit that stores identification data, and each die having an optical identification mark positioned thereon and encoding information corresponding to the identification data, optical identification mark on each die being accessed through a lookup table to correspond to the electronic identification information.

11. The wafer of claim 10 wherein the programmable identification circuit includes a plurality of programmable links.

12. The wafer of claim 10 wherein the optical identification mark encodes information identical to the identification data.

13. The wafer of claim 10 wherein the identification data uniquely distinguishes each of the dies.

14. A plurality of integrated circuit chips, each comprising:

a housing;

an integrated circuit enclosed within the housing and including an identification circuit that stores identification data distinguishing each of the integrated circuit chips from one another; and

an optical mark positioned on an exterior surface of the housing and encoding identification information being accessed through a lookup table to correspond to the identification data.

15. The integrated circuit chips of claim 14, further comprising electrical contacts connected to said housing and adapted to provide electrical connection between the integrated circuit and circuitry external to the housing.

16. The integrated circuit chips of claim 14 wherein the optical mark is a first optical mark encoding first identification information, and further comprising a second optical mark positioned on the integrated circuit enclosed within the housing and encoding second identification information corresponding to the identification data.

17. The integrated circuit chips of claim 16 wherein the first identification information is identical to the second identification information.

18. The integrated circuit chips of claim 14 wherein the identification information is the same as the identification data.

19. A method of identifying a plurality of substantially identical integrated circuits formed on a common substrate, each of the integrated circuits being formed on a respective one of a plurality of substrate dies, the method comprising:

programming each of the plurality of integrated circuits with respective electronic identification information for each of the integrated circuits; and

marking each of the dies with optical identification code which corresponds with the respective electronic identification information;

reading the optical identification code on each of the integrated circuits;

reading the electronic identification information from each of the integrated circuits; and

accessing a lookup table to associate the optical identification code on each of the integrated circuits with the corresponding electronic identification information.

20. The method of claim 19 wherein the electronic identification information is distinct for each of the integrated circuits.

21. The method of claim 19 wherein the optical identification code is distinct for each of the dies.

22. The method of claim 19 wherein the optical identification code and the electronic identification information include identical data.

23. A method of identifying an integrated circuit, comprising:

programming the integrated circuit with an electronic identification information; and

marking the integrated circuit with an optical identification code that corresponds with the electronic identification information;

reading the electronic identification information; and

cross-referencing the optical identification code with the read electronic identification information to associate the optical identification code with the corresponding electronic identification information.

24. The method of claim 23 wherein the act of cross-referencing the optical identification code with the read electronic identification information comprises:

reading the optical identification code; and

cross-referencing the read optical identification code with the read electronic identification information.

25. The method of claim 23 wherein the act of cross-referencing the optical identification code with the read electronic identification information comprises accessing a lookup table containing the optical identification code and the read electronic identification information.

26. The method of claim 23 wherein the act of programming the integrated circuit with electronic identification information comprises programming at least one of a plurality of programmable links.

27. The method of claim 23 wherein the act of marking the integrated circuit with an optical identification code includes the step of placing an adhesive label on the integrated circuit.

28. In an integrated circuit which includes a programmable circuit for storing an electronically readable identification code which identifies the integrated circuit, a method of identifying the integrated circuit, comprising the steps of:

marking the integrated circuit with an optical identification code;

reading the electronically readable identification code; and

comparing the optical identification code with the read electronically readable identification code to associate the optical identification code with the electronically readable identification code.

29. The method of claim 28 wherein the act of comparing the read electronically readable identification code with the optical identification code comprises:

creating a look-up table that associates the optical identification code for each of a plurality of integrated circuits with an optical identification code; and

accessing the look-up table.

30. The method of claim 29 wherein the act of creating a look-up table that associates the optical identification code for each of a plurality of integrated circuits with an optical identification code comprises creating a look-up table that uniquely associates the optical identification code for each of a plurality of integrated circuits with an optical identification code.

31. The method of claim 29 wherein the act of creating a look-up table that associates the optical identification code for each of a plurality of integrated circuits with an

optical identification code comprises creating a look-up table that uniquely associates the optical identification code for each of a plurality of integrated circuits with an optical identification code.

32. An integrated circuit comprising an integrated circuit chip mounted within a package, the integrated circuit comprising:

an identification circuit fabricated on the integrated circuit chip, the identification circuit being operable to store identification data; and

an optical identification mark on the package of the integrated circuit, the optical identification mark encoding information corresponding to the identification data.

33. The integrated circuit of claim 32 wherein the programmable identification circuit includes a plurality of programmable links.

34. The integrated circuit of claim 33 wherein the optical identification mark encodes information identical to the identification data.